REMARKS

Present Status of the Application

The Office Action rejected claims 1-9 under 35U.S.C 112, first paragraph, as failing to comply with the written description requirement. The Office Action also rejected claims 10-17 under 35 U.S.C. 103(a), as being unpatentable over Russ et al. (U.S. 2003/0047750) in view of Amerasekera (EP 0822 596).

Applicant has amended claim 1 to more clearly define the invention. After entry of the foregoing amendments, claims 1-17 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Claims 1-9 rejected under 35 U.S.C 112, first paragraph

The Office Action rejected claims 1-9 under 35U.S.C 112, first paragraph, as failing to comply with the written description requirement, because the newly added limitation "the dopant concentration of the second conductive type embedded region under the second conductive type well is the same to the dopant concentration of the second conductive type embedded region beside the second conductive type well" is not disclosed in the original specification including original claims.

Applicant respectfully traverses the rejection because the newly added limitation "the dopant concentration of the second conductive type embedded region under the second conductive type well is the same to the dopant concentration of the second conductive type embedded region beside the second conductive type well" in claim 1 is canceled.

Claims 1-9 rejected under 35 U.S.C 102 (b)

The Examiner rejected claims 1-9 under 35 U.S.C 102(b) as being anticipate by Russ et al. (U.S. 2003/0047750)in the final Office Action dated on 09/30/2005. Applicant respectfully traverses the rejections for at least the reasons set forth below.

The present invention is in general related a junction diode as claim 1 recites:

Claim 1. A junction diode, comprising:

a first conductive type substrate;

a second conductive type embedded region, formed within the first conductive type substrate;

a second conductive type well, formed within the second conductive type embedded region, wherein the second conductive type well has a dopant concentration smaller than the second conductive type embedded region, and the second conductive type embedded region surrounds the second conductive type well;

one first conductive type doped region, formed in the second conductive type well; and

two second conductive type doped regions, formed in the second conductive type embedded region beside the first conductive type doped region.

In the Russ reference, as shown in Fig. 2,there are two P+ regions 212_1, 212_2 in the N-epi layer 208 such that ***the P+region 212_1, the N-epi layer 208 and the P+ regions 212_2 form a lateral PNP transistor*** of a SCR (see abstract). However, in claim 1 of the present invention, ***only one first conductive type doped region is formed in the second conductive type well,*** such that a PN junction diode is formed. In the present invention, the PN junction diode is used as an ESD circuit. Because the PN junction diode occupies a smaller area and has a smaller capacitance, the junction diode has very little effect on the performance of a RF circuit. On the contrary, in the Russ reference, the SCR of the ESD protection device is composed of two the P+ regions 212_1, 212_2 and the N-epi layer 208. It would occupy a larger area apparently, and a larger capacitance may be existed. Therefore, this design of the SCR is not suitable using in a RF circuit because the performance of a RF circuit will be affected by the existed capacitance from the SCR.

Applicant respectfully submits that Russ fails to teach or suggest that only one first conductive type doped region is formed in the second conductive type well. Therefore, Russ does not teach each and every element in claim 1. In order to properly anticipate Applicants' claimed invention under 35 U.S.C 102, each and every element of claim in issue must be found, "either expressly or inherently described, in a single prior art reference". "The identical

invention must be shown in as complete details as is contained in the .... claim. Richardson v. Suzuki Motor Co., 868 F. 2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989)." See M.P.E.P. 2131, 8th ed., 2001.

For at least the foregoing reasons, Applicant respectfully submits that independent claim 1 patently define over the prior art reference, and should be allowed. For at least the same reasons, dependent claims 2-9 patently define over the prior art as a matter of law, for at least the reason that these dependent claims contain all features of their respective independent claim 1.

Claims 10-17 rejected under 35 U.S.C 103 (a)

The Office Action rejected claims 10-17 under 35 U.S.C. 103(a), as being unpatentable over Russ et al. (U.S. 2003/0047750) in view of Amerasekera (EP 0822 596). In particular, the Office Action pointed out the diode of claim 10 comprises:

a first conductive type substrate;

a second conductive type embedded region;

a second conductive type epitaxial well;

a first conductive type doped region; and

at least two second conductive type regions. (see page 4 of the office action)

However, applicant respectfully submits the Examiner misunderstands claim 10 because claim 10 is described as below:

10. A junction diode, comprising:

a first conductive type substrate;

a second conductive type deep well, formed within the first conductive type substrate;

a first conductive type well, formed within the second conductive type deep well;

a first conductive type shallow well, formed within the first conductive type well, wherein the first conductive type shallow well has a dopant concentration smaller than the first conductive type well;

a plurality of first conductive type doped regions, formed in the first conductive type well; and

a plurality of second conductive type doped regions formed in the second conductive type deep well and one second conductive type doped region formed in the first conductive type shallow well, wherein the second conductive type doped region formed in the first conductive type shallow well is isolated from the second conductive type deep well by the first conductive type well and the first conductive type shallow well.

Therefore, applicant respectfully requests to withdraw the 103(a) rejection.

In addition, the two references (Russ and Amerasekera) combined apparently fail to teach or suggest each and every element in claim 10. Hence, independent claim 10 patently define over the prior art references, and should be allowed. For at least the same reasons, dependent claims 11-17 patently define over the prior art as a matter of law.

Claims 1-9 are patently define over the prior art references

In the Office Action, the Examiner rejected the diode comprising a first conductive type substrate; a second conductive type embedded region; a second conductive type epitaxial well; a first conductive type doped region; and at least two second conductive type regions, ***which is the subject matter of claim 1,*** under 35 U.S.C. 103(a) as being unpatentable over Russ et al. (U.S. 2003/0047750) in view of Amerasekera (EP 0822 596). Applicant respectfully traverses the rejection of claims 1-9 under 103(a) as being unpatentable over Russ in view of Amerasekera because a prima facie case of obviousness has not been established by the Office Action.

The present invention provides a junction diode as claim 1 recites:

Claim 1. A junction diode, comprising:

a first conductive type substrate;

a second conductive type embedded region, formed within the first conductive type substrate;

a second conductive type well, formed within the second conductive type embedded region, wherein the second conductive type well has a dopant concentration smaller than the

second conductive type embedded region, and the second conductive type embedded region surrounds the second conductive type well;

one first conductive type doped region, formed in the second conductive type well; and two second conductive type doped regions, formed in the second conductive type embedded region beside the first conductive type doped region.

As discussed above mentioned, Russ fails to teach or suggest that only one first conductive type doped region is formed in the second conductive type well. Amerasekera also fails to teach or suggest that only one first conductive type doped region is formed in the second conductive type well. In the Amerasekera reference, as shown in Fig. 1b, a N+ region 7 and a P+ region 15 is formed in the P-well 5 which is formed in the N-well 3. However, in claim 1 of the present invention, only one first conductive type doped region is formed in the second conductive type well, such that a PN junction diode is formed. In the present invention, the PN junction diode is used as an ESD circuit. Because the PN junction diode occupies a smaller area and has a smaller capacitance, the junction diode has very little effect on the performance of a RF circuit.

Therefore, Russ and Amerasekera combined do teach each and every element in claim 1, and thus a prima facie case of obviousness has not been established. To establish a prima facie case of obviousness under 35 U.S.C. 103(a), each of three requirements must be met. First, the reference or references, taken alone or combined, must teach or suggest each and every element in the claims. Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skilled in the art, to combine the references in a manner resulting in the claimed invention. Third, a reasonable expectation of success must exist. Moreover, each of the three requirements must " be found in the prior art, and not be based on applicant's disclosure." See M.P.E.P. 2143, 8th ed., February 2003.

For at least the foregoing reasons, Applicant respectfully submits that independent claim 1 patently define over the prior art references, and should be allowed. For at least the same reasons, dependent claims 2-9 patently define over the prior art as a matter of law.

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CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 1-17 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
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